Bio-Data

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OBJECTIVE

Willingness for sharing experience with peer in academia/industry/research

PROFILE

Strong academic background

Has demonstrated ability to pursue independent research along-with academic career

EDUCATION

Indian Institute of Technology, Delhi
Ph. D. EE (VLSI Design) **2001**
Dissertation: "VLSI Design Processes: Modeling & Improvement"

Indian Institute of Technology, Delhi
M. Tech. Integrated Electronics & Circuits **1989**
Thesis: "Chip realization of efficient pattern recognition circuits"

National Institute of Technology, Jaipur
B. E. Electronics & Comm. Engineering **1987**
Thesis: "Microprocessor based instrumentation system for control & performance evaluation of an induction motor"
Degree passed in "I division with Honors"

RECOGNITIONS, HONORS & AWARDS

- Fellow of IETE India **2002**
- Senior of IEEE USA, Computer Society **2004**
- Member, sub-committee on "Curriculum development" for the "Education & awareness in Information Security" project sponsored by Ministry of Comm. & IT, Government of India **2004**
- Visiting faculty, Microelectronics programme at Asian Institute of Technology Thailand **2004**
- Fellow of Institution of Engineers, India (Computer stream) **2008**
- Fellowship Chair, 22nd IEEE International Conference on VLSI Design, New Delhi **5 -9 January 2008**

TEACHING EXPERIENCE

National Institute of Technology, Jaipur **2001-2010**
Assoc. Prof– Dept. of ECE
Post Ph.D. experience of 7 years
Developed curriculum/syllabus and overall course structure, proposed new lab courses.

National Institute of Technology, Jaipur **1990-2001**
Assistant Prof.- Dept. of ECE
Revised syllabus and lab course structuring.

RELATED EXPERIENCE

Dept. of EE, Indian Institute of Technology, Delhi
Honorary Research Assistant/teaching assistant **1998-2000**
Sponsored project by Motorola USA on "Design flow for electronic products design" Proposed and implemented a new modeling and improvement approach for concurrent design processes.

Under Prof. C. P. Ravikumar

CARE, Indian Institute of Technology, Delhi
Honorary Research Assistant **1988-89**
Sponsored project by DOE, Govt. of India
Successfully realized two chips for efficient pattern recognition using VTI CAD tools on SUN workstations

Under Dr. Navneet Jain

PUBLICATIONS AND RESEARCH REALTED ACTIVITIES

- 04 papers published in journals & 35+ papers published in international and national refereed/open conferences
- Published four technical reports
- Completed two funded research projects
- Two lab monographs, available for in-house use at MNIT Jaipur
- Guiding five doctoral dissertations, two completed
- Guided 30+ postgraduate dissertations, several undergraduate theses
- Designed undergraduate/postgraduate courses & schemes of various universities
- Doctorate theses examiner for various central universities

LANGUAGES

- English – speak fluently and read/write with high proficiency
- French – speak, read, and write with basic competence

MEMBERSHIPS & PROFESSIONAL AFFILIATIONS

- Life Fellow, IETE, India
- Senior Member, IEEE-Circuits & Systems society & Computer Society
- Life member, International Microelectronics & Packaging Society, India chapter
- Life member, Indian Society for Technical Education
- Member, VLSI Society of India
- Life Fellow, IE India (Computer stream)
- Member, IAENG
- Member of technical programme committee
  - DATICS conference 2010
  - IE National Seminar on Advanced Electronic Systems- Modeling & Simulation, Aug. 2008
  - VDAT workshops 1998-2010
  - IETE Zonal seminar on “Electronic Design Automation” 2003 Jaipur India
  - VLSI Education Workshop 2005
- Member of review management committee
  - ISCAS 2005 Japan
  - ISCAS 2006 Greece
  - VDAT Symposium 2005-2010
  - SCI 2003, 2004
- Has chaired sessions at *International Conf. on VLSI Design*, *ASP-DAC*, *VDAT, ISCAS* & other conferences
- Has been reviewing for many reputed conferences

COMMUNITY INVOLVEMENT

- Member, Institution of Engineers (India) Rajasthan section **2008-09**
- Hony. Treasurer, IETE Rajasthan section **2004-06**
- Hony. Organizing Secy., Rajasthan Viklang Vikas Society **2003-05**
- Has organized four national workshops as principal chair, and four others as organizing committee member
- Has been finance co-chair, VLSI Design & Test Symposium **1998-2000**
- Has organized four teachers’ training programme & instruction enhancement programme in the field of VLSI
- Has been faculty coordinator, Campus-LAN & Internet, MNIT Jaipur **2003-06**
- Centre observer, Rajasthan PET **2001, 2002**
- Has delivered 30+ invited/technical talks at teachers’ training programme, technical festivals and other technical meets

AREAS OF INTEREST & EXPTERTISE

- VLSI Design process improvement & management; High level design, modeling & synthesis; Analog synthesis & interconnect modeling; Formal verification of digital hardware.

PREVIOUS FOREIGN-VISITS

- Asian Institute of Technology, Bangkok, as visiting faculty during fall semester 2004 (03months)
- Tallinn, ESTONIA, to attend 26th IEEE International Conference- NORCHIP, November 2008 (03 days)
- North Dakota State University, for research collaboration, 23-27 March 2009
- Singapore, to attend Region 10 Annual International conference TENCON, Dec. 2009